AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 2, line 8, with the following rewritten paragraph:

The operation of the Pixel Block is as follows: Node IN is connected to switch RES, the cathode of photodiode ~~photofiode~~ PD, and the gate of NMOS transistor N1. Initially switch RES is closed and the voltage on node IN is VRES. Then switch RES is opened. There will be a finite charge on node IN dependent on the voltage VRES, the capacitance of photodiode PD, and the gate capacitance of NMOS transistor N1. The photodiode current causes the charge on node IN to be discharged and the voltage on node IN decreases. Generally imagers have a fixed integration time or period. The voltage on node IN at the end of the integration period is referred to herein as VPD.